

WHAT IS CLAIMED IS:

- 1 1. A clock filter for an electronic device, the clock filter comprising:
2 a clock receiver electrically coupled to an external clock; and
3 an enabling circuit electrically coupled to the clock receiver;
4 wherein the clock receiver generates an internal clock signal and the enabling
5 circuit disables the clock receiver for a first time period after detecting a transition on the
6 internal clock signal.
- 1 2. The clock filter of claim 1, wherein the enabling circuit includes a pulse
2 generator.
- 1 3. The clock filter of claim 2, wherein the pulse generator is electrically coupled to
2 the clock receiver, and the pulse generator generates a pulse signal having a duration
3 substantially equivalent to the first time period.
- 1 4. The clock filter of claim 3, wherein the clock receiver is disabled when the pulse
2 signal is high.

1 5. The clock filter of claim 1, wherein the enabling circuit is electrically coupled to a
2 clock filter enable signal.

1 6. The clock filter of claim 5, wherein the enabling circuit disables the clock receiver
2 when the clock filter enable signal is enabled.

1 7. A clock filter for an electronic device, the clock filter comprising:
2 a clock receiver electrically coupled to an external clock signal, the clock receiver
3 generating an internal clock signal;
4 a pulse generator electrically coupled to the clock receiver, the pulse generator
5 generating a pulse signal for a first time period after detecting a transition in the internal
6 clock signal; and
7 an enabling circuit electrically coupled to the pulse generator and the clock
8 receiver, the enabling circuit being electrically coupled to a clock filter enable signal and
9 disabling the clock receiver when the clock filter enable signal is enabled during the first
10 time period.

1 8. The clock filter of claim 7, wherein the enabling circuit is electrically coupled to a
2 clock enable signal, the enabling circuit disabling the clock receiver when the clock
3 enable signal is reset.

1 9. The clock filter of claim 7, wherein the enabling circuit includes:
2 a NAND gate electrically coupled to the pulse generator and the clock filter
3 enable signal; and

4 an AND gate electrically coupled to the NAND gate such that the output of the
5 NAND gate is a first input to the AND gate.

1 10. The clock filter of claim 9, wherein the AND gate has a second input electrically
2 coupled to a clock enable signal.

1 11. The clock filter of claim 9, wherein an output of the AND gate is electrically
2 coupled to the clock receiver.

1 12. The clock filter of claim 7, wherein the enabling circuit includes:
2 a first NAND gate electrically coupled to the pulse generator and the clock filter
3 enable signal;
4 a second NAND gate electrically coupled to the output of the first NAND gate;
5 and
6 an inverter electrically coupled to the output of the second NAND gate, wherein
7 the output of the inverter is electrically coupled to the clock receiver.

1 13. The clock filter of claim 12, wherein the second NAND gate has a second input
2 electrically coupled to a clock enable signal.

1 14. The clock filter of claim 12, wherein the first NAND gate has a second input
2 electrically coupled to a test mode enable signal.

1 15. The clock filter of claim 7, wherein the first time period is about 5% to about 10%
2 of a transition period of the external clock signal.

1 16. A method of generating an internal clock signal, the method comprising:
2 receiving an external clock signal;
3 setting an internal clock signal high when the external clock signal is above a first
4 threshold;
5 setting the internal clock signal low when the external clock signal is below a
6 second threshold; and
7 maintaining the internal clock signal in a constant state for a first time period after
8 the internal clock signal transitions from high-to-low or from low-to-high.

1 17. The method of claim 16, wherein the first threshold is approximately one-half of a
2 reference voltage.

1 18. The method of claim 16, wherein the second threshold is approximately one-half
2 of a reference voltage.

1 19. The method of claim 16, wherein the first time period is about 5% to about 10%
2 of a transition period of the external clock signal.

1 20. The method of claim 16, wherein the step of maintaining is performed only when
2 a clock filter enable signal is enabled.

1 21. The method of claim 20, wherein further comprising:
2 receiving one or more of a first command;
3 receiving one or more of a second command after receiving one or more of the
4 first command with no intervening commands; and
5 enabling the clock filter enable signal after receiving one or more of the second
6 command.